UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,407	01/15/2004	Yuuichi Hirano	247632US	4934

22850 7590 04/05/2005

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/757,407	HIRANO ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/778,104.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the preliminary amendment file January 15, 2004.

Priority

This application filed under former 37 CFR 1.60 lacks the necessary reference to the prior application. A statement reading "This is a Divisional of Application No. 09/778,104, filed February 7, 2001, Now US Patent 6,787,855." should be entered following the title of the invention or as the first sentence of the specification. Also, the current status of all nonprovisional parent applications referenced should be included.

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/778,104, filed on February 7, 2001.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Wada (5,859,466).

Wada teaches a semiconductor device comprising:

a substrate 7;

a transistor 1 having a pair of source/drain regions 2 & 3 formed in the substrate 7 and a gate electrode 4 formed via a gate dielectric film 9 on a channel region sandwiched between the pair of source/drain regions 2 & 3;

an interlayer dielectric film 13 formed on the transistor 1;

source/drain wirings 16 & 17 (portions formed above interlayer dielectric film 13) formed on the interlayer dielectric film 13; and

conductors 16 & 17 (portions formed within the openings) formed in the interlayer dielectric film 13 for connecting the source/drain wirings 16 & 17 (portions formed above interlayer dielectric film 13) to the source/drain regions 2 & 3, wherein

the interlayer dielectric film 13 is formed except for a region between the gate electrode 4 and the conductors 16 & 17 (portions formed within the openings) (Figure 1A, column 4, lines 6-36).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Segawa et al. (US 6,603,172 B1) in view of Yu (US 6,194,748 B1).

Segawa et al. teach a semiconductor device comprising:

a substrate 1;

a transistor having a pair of source/drain regions 10 formed in the substrate, a gate electrode 6a formed via a gate dielectric film 5a on a channel region sandwiched between the pair of source/drain regions 10, and a side wall 8 formed on a side surface of the gate electrode 6a;

an interlayer dielectric film formed on the transistor;

source/drain wirings 14 formed on the interlayer dielectric film; and

conductors 13b formed in the interlayer dielectric film for connecting the source/drain wirings 14 to the source/drain regions 10 (Figures 5(a)-5(e).

However, Segawa et al. fail to teach the transistor formed in the substrate and the side wall constructed with a porous material.

Yu teaches a transistor 12 formed in a substrate 14 (Figure 1, column 3, lines 18-19) and a side wall 38 constructed with a porous material (Figure 1, column 7-8, lines 4-8 and 13-14, respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device structure as taught by Segawa et al. with the semiconductor device having transistor formed in a substrate and a side wall constructed with a porous material as taught by Yu to provide a semiconductor device capable of reducing the gate-edge fringing capacitance (column 4, lines 30-33).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to claimed semiconductor device:

Choi et al. (5,801,416)	Gardner et al. (6,018,179)
Hsu et al. (5,705,839)	Kim (5,955,746)
Ma et al. (5,939,753)	Matsuoka (6,081,007)
Morihara et al. (US 6,271,564 B1)	Oda et al. (US 6,469,347 B1)
Ogawa (US 6,380,584 B1)	Oyamatsu (US 6,204,539 B1)
Takao (US 6,215,138 B1)	Yamamoto et al. (US 6,359,318 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
April 1, 2005